ABSTRACT OF THE DISCLOSURE

The present invention provides a method of manufacturing a multilayer semiconductor structure featuring reduced ohmic losses with respect to standard multilayer semiconductor structures. The semiconductor structure comprises a high resistivity silicon substrate with resistivity higher than 3 KΩ.cm, an active semiconductor layer and an insulating layer in between the silicon substrate and the active semiconductor layer. The method comprises suppressing ohmic losses inside the high resistivity silicon substrate by increasing, with regard to prior art devices, charge trap density between the insulating layer and the silicon substrate. In particular this may be obtained by applying an intermediate layer in between the silicon substrate and the insulating layer, the intermediate layer comprising grains having a size, wherein the mean size of the grains of the intermediate layer is smaller than 150 nm, preferably smaller than 50 nm.